AMENDMENTS TO THE DRAWINGS

The accompanying Replacement sheets of drawings include changes to the drawings, and replace the original sheets of drawings of Figures 1-3. Descriptive labels have been added to all boxes, and no new matter has been added. Approval and entry are respectfully requested.

REMARKS

Claims 16-22 have been added, and therefore claims 1-22 are pending.

Applicant thanks the Examiner for acknowledging receipt of the previously filed papers, and for confirming that certified copies of the priority documents have been received.

In view of the following, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

With respect to paragraph four (4) of the Office Action, the drawings were objected to as lacking labels. The drawings have been amended accordingly. Approval and entry are respectfully requested.

With respect to paragraph five (5) of the Office Action, the title was objected to for not being descriptive. Applicant respectfully traverses the objection and with the recommendation for a new title. Applicant submits that the present title is descriptive of the presently claimed subject matter. The title must be as short and specific as possible. M.P.E.P. ' 606. The title proposed by the Examiner, "METHOD FOR CONTROLLING THE PROGRAM RUN IN A MICROCONTROLLER BASED ON INFORMATION STORED IN ANOTHER COMPONENT OR MICROCONTROLLER", apart from being quite long, refers only to the case of at least one microcontroller and one component, or two microcontrollers, whereas claim 1 includes the case of a single microcontroller with no additional components.

With respect to paragraph seven (7) of the Office Action, claims 3 and 6-9 were rejected under 35 U.S.C. ' 112, second paragraph, as indefinite.

Applicant thanks the Examiner for identifying formal inconsistencies in claims 3 and 6. The claims have been amended to correct the inconsistencies. Claim 7 has also been amended to correct a typographical error. No new matter has been added, and no change in claim scope or surrender of claimed subject matter is intended. Approval and entry are respectfully requested.

Claim 3 has been corrected so that the "additional microcontroller" has proper antecedent basis.

Claim 6 has been corrected so that the "microcontroller" has proper antecedent basis. The term "another program" in claim 6 has been changed to "a program sequence". The Office Action also objected to the use of the term "computing element" and recommended replacing it with "microprocessor," but it is submitted that a computing element is an element that can perform a computation, in particular run a program. The computing element in claim 6 is the element that runs the program sequence as supported

in the specification (page 6, lines 1-4). It is therefore submitted that to replace "computing element" with "microprocessor", as suggested by the Examiner, may create ambiguity.

Claims 7-9 were objected to only for being dependent from claim 6 that was objected to, and are therefore proper in view of the foregoing.

With respect to paragraph twelve (12) of the Office Action, claims 1-3, 6-7 and 10-14 were rejected under 35 U.S.C. ' 102(b) as anticipated by U.S. Patent No. 4,933,941 to Eckard et al. ("Eckard"). The rejections should be withdrawn for at least the following reasons.

The "Eckard" reference refers to an apparatus for testing a central processing unit (CPU) 10. The apparatus includes an auxiliary processor 21 and an auxiliary memory 22, the auxiliary memory storing a test program. When the apparatus detects that the CPU is in an idle state, or when a predetermined amount of time has elapsed since the last test, the CPU 10 transfer control to the auxiliary processor 21, which saves the state of the CPU, causes the CPU to run the test program, compares the results with reference results, restores the state of the CPU, and returns control to the CPU. The test mode register 23 provides status information with respect to the operation of the test program.

It is respectfully submitted that the rejections may be based on a misinterpretation of the presently claimed subject matter.

To anticipate a claim under § 102(b), a single prior art reference must identically disclose each and every claim feature M.P.E.P. § 2131. Claim 1 is to a method for controlling a run of a *program* executable on at least one *microprocessor* of *a microcontroller*, including the steps of: reading in *information regarding a hardware of the microcontroller* from at least one *information register* of the microcontroller; and *actuating* at least one *switch* via which the program run is *controlled* as a function of the information read in.

(Emphasis added.) The Office Action apparently suggests the following correspondences of claim 1 to "Eckard": *program* = test program; *microprocessor* = auxiliary processor 21; *microcontroller* = elements 21, 22, 23 and 105; *information regarding a hardware of the microcontroller* = status information; *information register* = test mode register 23; *actuating* = flipping of bits from 0 to 1 and vice versa; *switch* = bit of the test mode register 23; *controlled* = started, stopped, etc, which are not supported for the following reasons.

The Office Action suggests that the test program runs on the auxiliary processor 21. However, it is clear from the "Eckard" disclosure that the test program runs on the CPU 10 and not on the auxiliary processor 21. See for example col.5, lines 6-10: "In step 404, the auxiliary processor 21 initiates the operation of the central processing unit 10, the central processing unit 10 executing the test program sequence supplied from the auxiliary

memory 22." Therefore the correspondence between the microprocessor of claim 1 and the auxiliary processor 21 lacks support in the "Eckard" reference.

The Office Action also suggests that the "information regarding a hardware of the microcontroller" is the status information of "Eckard", and that the "information register" is the test mode register 23 of "Eckard", but, it was shown above that the microcontroller of claim 1 cannot be the auxiliary processor 21 of "Eckard". The test mode register 23 does not contain information regarding a hardware of the CPU 10.

Moreover, the Office Action may have misinterpreted the term "information regarding a hardware" as used in the present application. The specification (page 4, lines 9-10) provides that the information to be read in, regarding the microcontroller includes, for example, the manufacture, model, type and size of the components used for the microcontroller." The information contained in the test mode register of "Eckard" concerns the status of the test operation *and not the hardware.* The "Eckard" reference does not identically describe (or even suggest) "reading in information regarding a hardware of the microcontroller."

Claim 1 provides the feature of "actuating at least one switch as a function of the information read in". The Office Action suggests that the "switch" of claim 1 is a bit in the test mode register 23 of "Eckard", and that "actuating" is the flipping of this bit from 0 to 1 and vice versa. However, the "Eckard" reference refers only briefly the function of the test control register. The only function expressly stated is to "provide status information" (col.4, lines 40-42). From this description it appears that the test mode register is essentially an output device with no control purposes. In particular, the "Eckard" reference does not identically describe (or even suggest) *actuating* the bits of the test mode register. The text of col. 5, lines 44-61, of "Eckard" concerns the function of each bit in the test mode register, but nothing identically describes (or even suggests) that these bits can be set to affect the execution of the test program.

More generally, it seems that according to the Office Action's interpretation, the test mode register 23 should perform double duty, as an *information register* and as a *switch*. This would imply that information is first obtained from the test mode register, and then the register is modified to control the test program. This would require a nonobvious sequence of steps that is not described (or even suggested) by the "Eckard" disclosure.

Finally, the Office Action seems to suggest that the term "controlled" in claim 1 corresponds to the starting and stopping of the test program in "Eckard". The specification of the present application (page 4,lines 5-7) provides that "Specific switches are then set as a function of the acquired hardware information in such a manner that certain workarounds and program features are activated or deactivated. The program run

is, therefore, adapted to the hardware of a microcontroller."

Claim 6, as presented provides the feature of "a storage medium storing a program sequence that can be executed on a computing element, the program sequence causing the computing element to: read in *information regarding a hardware of the microcontroller* from at least one *information register* of the microcontroller, and *actuate* at least one *switch* via which a program run is *controlled* as a function of the information read in." The same remarks made as to claim 1 also apply to claim 6.

Moreover, the Office Action suggests that the "storage medium" of claim 6 is the auxiliary memory 22 of "Eckard". However claim 6 provides the feature of "a storage medium storing a program sequence ... the program sequence causing the computing element to: read in information regarding a hardware ... actuate at least one switch via which a program run is controlled ." The auxiliary memory 22 of "Eckard" *stores* a test program. However the steps of reading the hardware information and actuate the switch amount to *controlling* the test program. In short, the Office Action is suggesting that the test program *controls itself*, which is not taught or even suggested by "Eckard."

Claim 10 provides for a *microcontroller*, including: at least one *microprocessor* including a *program* that is executable on the at least one microprocessor; at least one *information register*; an arrangement for reading in *information regarding a hardware of the microcontroller* from the at least one information register; and at least one *switch actuatable* as a function of the information read in and for *controlling* a run of the program executable on the at least one microprocessor." The same remarks made in reference to claim 1 apply to claim 10, in particular regarding the lack of correspondence between the italicized terms of claim 10 and the elements of the "Eckard" reference.

Based on the foregoing remarks, the "Eckard" reference does not anticipate the subject matter of claim 1, 6 and 10, and claims 2-3, 7 and 11-14 depending therefrom for the reasons explained.

For at least the foregoing reasons, claims 1-3, 6-7 and 10-14 are allowable.

With respect to paragraph twenty-three (23) of the Office Action, claims 1 and 4 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,175,913 to Chesters et al. ("Chesters"). The rejections should be withdrawn for at least the following reasons.

The "Chesters" reference refers to a data processing unit with built-in debug capabilities. A bus control unit 12 monitors usage of the bus 13 by the CPU 7 or the DMA unit 8 and generates signals that control the run of a program on CPU 7 when, for example, instructions or data at certain memory addresses are read or written. Address ranges are defined for example by registers 15-18, while mode registers 15a and 17a control how those ranges are protected or whether breakpoints should be set.

To anticipate a claim under § 102(b), a single prior art reference must identically disclose each and every claim feature M.P.E.P. § 2131. Claim 1 provides the feature of "reading in *information regarding a hardware of the microcontroller* from at least one *information register* of the microcontroller; and *actuating* at least one *switch* via which the program run is controlled *as a function of the information read in"* (emphasis added). The Office Action suggests that the *information register* of claim 1 is one of the registers 15-18 of "Chesters", and that the *information regarding a hardware of the microcontroller* is an information about the memory.

As explained above in reference to the "Eckard" disclosure, registers 15-18 of "Chesters" only contain memory addresses of breakpoints and debug variables which are *set by a user* according to the user's debug strategy, and registers do not contain any *information about the hardware of the microcontroller.* Since the addresses contained in registers 15-18 are arbitrarily assigned by a user or by external debug hardware, they don't even need to be *legal* addresses, therefore they do not tell anything about the memory they refer to. The "Chesters" reference does not disclose (or even suggest) "reading in information regarding a hardware of the microcontroller".

Regarding the *switch* of claim 1, the Office Action seems to refer to the mode registers 15a and 17a. The mode registers 15a, 17a are input registers used to set breakpoints, etc. These registers can also be set by a user, or by external debug hardware according to the user's debug strategy. The "Chesters" reference does not disclose (or even suggest) "actuating at least one switch via which the program run is controlled as a function of the information read in".

The "Chesters" reference does not anticipate the subject matter of claim 1 and claim 4 depending therefrom. Therefore claims 1 and 4 are allowable.

With respect to paragraph twenty-seven (27) of the Office Action, claim 5 was rejected under 35 U.S.C. § 103(a) as unpatentable over "Chesters" in view of U.S. Patent No. 6,182,203 to Simar Jr. et al. ("Simar"). Claim 5 depends from claim 4 which has been shown to be allowable. Therefore claim 5 is similarly allowable, since the secondary reference does not cure the critical deficiencies of the primary reference.

With respect to paragraph thirty-two (32) of the Office Action, claim 8 was rejected under 35 U.S.C. § 103(a) as unpatentable over "Eckard" in view of IEEE Dictionary. Claim 8 depends from claim 6 and is therefore similarly allowable, since the secondary reference does not cure the critical deficiencies of the primary reference.

With respect to paragraph thirty-seven (37) of the Office Action, claims 9 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over "Eckard" in view of "Simar". Claims 9 and 15 depend from claims 6 and 14 and are therefore similarly allowable, since the secondary reference does not cure the critical deficiencies of the primary reference.

New claims 16-22 do not add any new matter and are supported by the present application, including the specification. Claims 16-22 depend from claims 1, 2, 6, 10 to 17, and are therefore allowable for the same reasons.

Accordingly, claims 1-22 are allowable.

CONCLUSION

In view of the above, it is respectfully submitted that all of the presently pending claims are allowable. It is therefore respectfully requested that the objections and rejections be withdrawn, since they have been obviated. All issues raised having been addressed, an early and favorable action on the merits is respectfully requested.

Respectfully Submitted,

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